REMARKS

Claims 1-9 are all the claims pending in the application.

Applicant's representative would like to thank the Examiner and the Examiner's Supervisor for courtesies extended in the productive personal interview, which was conducted at the USPTO on January 15, 2003.

In the interview, the Examiner agreed that the amendments of claims 1, 2, and 5 as submitted herewith overcome the § 112 rejections of claims 1-9. Therefore, Applicant submits that the § 112 rejections of claims 1-9 should be withdrawn.

Additionally, in the interview, the Examiner agreed that Toyoda (JP 05-166965) does not disclose all of the recitations of the claimed invention, based on the drawing figures and an automated English language translation of Toyoda. However, the Examiner indicted that a certified English language translation of Toyoda would be obtained by the USPTO to confirm this position.

We would like to thank the Examiner for the facsimile of February 10, 2003, providing us with a copy of the certified English language translation of the Toyoda reference, which was obtained by the USPTO. Additionally, Applicant's representative would like to thank the Examiner for courtesies extended in the additional telephone interview conducted on February 19, 2003, in which the certified English language translation of the Toyoda reference was discussed.

In the telephonic interview, the Examiner agreed that the certified English language translation of Toyoda confirms that the through holes of Toyoda are provided in the insulating substrate 44, not the signal lines or the ground plates. For example, Toyoda discloses that the insulating substrate 44 has several first through holes 56 (see Figure 2) for a signal line and several second through holes 58 (see Figure 1) for a ground (see, for example, page 7, numbered paragraph 0011, of the certified English language translation of Toyoda). Toyoda further discloses that conductors are disposed in the first and second through holes for connecting the surface-side signal lines to the back face-side signal lines, and the surface-side ground pattern to the back face-side ground pattern, respectively (see page 5, "Means to solve the problem", of the certified English language translation of Toyoda). Therefore, for at least the foregoing reasons, the Examiner agreed that Toyoda neither discloses nor suggests all of the recitations of the claimed invention, and accordingly, the rejections of claims 1-9 by Toyoda should be withdrawn.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned attorney at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,

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WASHINGTON OFFICE

23373
PATENT TRADEMARK OFFICE

Date: March 4, 2003

APPENDIX

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS:

The claims are amended as follows:

1. (Thrice Amended) A semiconductor integrated circuit comprising [a signal transmission line of] a microstrip structure comprising:

a signal line; and

a ground plate,

wherein at least one through hole is formed in said signal line, and an inner wall of said through hole is only directly [not] electrically connected to said signal line[and said ground plate].

2. (Thrice Amended) A semiconductor integrated circuit comprising [a signal transmission line patterns of] a microstrip structure comprising: [of]

a signal line; and

a ground plate,

wherein at least one through hole is formed in said ground plate, and an inner wall of said through hole is only directly [not] electrically connected to [said signal line and]said ground plate.

5. (Thrice Amended) A semiconductor integrated circuit comprising [a signal transmission line of] a microstrip structure comprising:

a signal line; and

a ground plate,

wherein at least one through hole is formed in [both of] said signal line [and said ground plate], and an inner wall of said through hole which is formed in said signal line is only directly [not] electrically connected to said signal line, and

wherein at least one through hole is formed in said ground plate, and an inner wall of said through hole which is formed in said ground plate is only directly electrically connected to [and] said ground plate.